What is claimed is:

1. A method for fabricating a gain cell on a semiconductor substrate, the method comprising the steps of:

forming a vertical write transistor having multiple sides, the vertical write transistor having a gate, a body region and first and second source/drain regions;

forming a vertical read transistor having multiple sides, the vertical read transistor having a body region and first and second source/drain regions, the vertical read transistor further having a gate region that couples to the second source/drain region of the vertical write transistor;

forming a charge storage node coupled to the second source/drain region of the vertical write transistor;

forming a write bit line that couples to the first source/drain region of the vertical write transistor;

forming a write wordline that couples to the gate region of the vertical write transistor;

forming a read bit line that couples to the first source/drain region of the vertical read transistor; and

forming a read wordline that couples to the second source/drain region of the vertical read transistor.

2. The method for fabricating a gain memory cell according to claim 1, wherein the step of forming a vertical write transistor having a second source/drain region further includes forming the second source/drain region to comprise the gate region of the vertical read transistor.

3. The method for fabricating a gain memory cell according to claim 1, wherein the step of forming a vertical write transistor includes forming a n-channel

MOSFET, and wherein the step of forming a vertical read transistor includes forming a p-channel JFET.

4. The method for fabricating a gain memory cell according to claim 1, wherein the step of forming the charge storage node includes forming the storage node such that the data state on the storage node controls the operation of the vertical read transistor.

5. The method for fabricating a gain cell according to claim 1 wherein the step of forming a read wordline comprises forming the vertical read wordline buried beneath the second source/drain region of the vertical read transistor.

6. The method for fabricating a gain cell according to claim 1 wherein the step of forming a write wordline and read bit line comprises forming the write wordline and read bit line on opposing sides of the first source/drain region of the vertical read transistor.

7. The method for fabricating a gain cell according to claim 1 wherein the step of forming the write bit line and read wordline comprises forming orthogonally to the write bit line and read wordline.

8. The method for fabricating a gain memory cell according to claim 1, wherein the step of forming the body region of the vertical write transistor comprises forming the first source/drain region of the vertical read transistor.

9. A method for fabricating a gain memory cell array on a semiconductor substrate, the method comprising the steps of:

forming multiple vertical pillars of single crystalline semiconductor material extending outwardly from the substrate, the pillars having multiple sides, each pillar

including a pair of transistors in the same pillar, each of the transistors having a body region, a gate region and first and second source/drain regions, and wherein the second source/drain region of a first transistor comprises the gate for a second transistor, and wherein the first source/drain region of the second transistor comprises the body region of the first transistor, the pillars forming an array of rows and columns;

forming a number of write wordlines, wherein each write wordline is coupled to the gates of the first transistors in a row of vertical pillars in the array;

forming a number of write bit lines, wherein each write bit line is coupled to the first source/drain regions of the first transistors in a column of vertical pillars in the array;

forming a charge storage node coupled to the second source/drain region of each first transistor in the array of vertical pillars;

forming a number of read bit lines, wherein each read bit line is coupled to the first source/drain regions of the second transistors in a row of vertical pairs in the array; and

forming a number of read wordlines, wherein each read wordline is coupled to the second source/drain regions of the second transistors in a column of vertical pillars in the array.

10. The method of fabricating a gain cell array according to claim 9, wherein the step of forming the first transistor comprises a write transistor, and wherein the step of forming the second transistor comprises a read transistor.

11. The method of fabricating a gain cell according to claim 10, wherein the step of forming the second source/drain region of a write transistor also comprises the gate region of the read transistor, and wherein the step of forming the body region of a write transistor also comprises the first source/drain region of the read transistor.

12. The method of fabricating a gain cell array according to claim 9, wherein forming the charge storage node includes structuring the storage node to control the operation of the second transistor.

13. The method of fabricating a gain memory cell array according to claim 9, wherein forming a number of read bit lines includes forming the number of read bit lines of heavily doped p+ type polysilicon, and wherein forming the number of write wordlines includes forming the number of write wordlines of heavily doped n+ type polysilicon.

14. A method for fabricating a gain memory cell array having a number of gain memory cells, the method comprising:

forming a number of vertical pillars having an array of rows and columns, each vertical pillar comprising a vertical write transistor and a vertical read transistor each having a body region, a gate region, and first and second source/drain regions;

forming a number of write wordlines, wherein each write wordline is coupled to the gates of the write transistors in one row of vertical pillars in the array;

forming a number of write bit lines, wherein each write bit line is coupled to the first source/drain regions of the write transistors in one column of vertical pillars in the array;

forming a number of charge storage nodes, wherein each charge storage node is coupled to the second source/drain region of each write transistor in the array of vertical pillars, and wherein a charge stored on each of the charge storage nodes controls a conductivity of each of the read transistors in the array of vertical pillars;

forming a number of indepedent read bit lines for nondestructive read operations, wherein each independent read bit line is coupled to the first source/drain regions of the read transistors in one row of vertical pillars in the array; and

forming a number of read wordlines, wherein each read wordline is coupled to the second source/drain regions of the read transistors in one column of vertical pillars in the array,

wherein each gain memory cell of the gain memory cell array has an area substantially equal to four lithographic features.

15. The method of claim 14, wherein the forming of the number of write wordlines comprises forming the number of write wordlines each to a thickness of less than or equal to one-third a minimum lithographic dimension, wherein each write wordline is coupled to the gates of the write transistors in one row of vertical pillars in the array.

16. The method of claim 14, wherein the forming of the number of vertical pillars having an array of rows and columns further comprises forming the second source/drain regions of the vertical write transistors to comprise the gate regions of the vertical read transistors.

17. The method of claim 14, wherein the forming of the number of vertical pillars having an array of rows and columns further comprises forming the body regions of the vertical write transistors to comprise the first source/drain regions of the vertical read transistors.

18. A method for fabricating a data storage device, the method comprising:

forming a memory array, wherein the forming of the memory array includes forming multiple vertical pillars of single crystalline semiconductor material extending outwardly from the substrate, the pillars having multiple sides, each pillar including a pair of transistors in the same pillar, each of the transistors having a body region, a gate region and first and second source/drain regions;

forming a number of write wordlines, wherein each write wordline is coupled to the gates of the first transistors in a row of vertical pillars in the array;

forming a number of write bit lines, wherein each write bit line is coupled to the first source/drain regions of the first transistors in a column of vertical pillars in the array;

forming a number of charge storage nodes coupled to the second source/drain region of each first transistor in the array of vertical pillars;

forming a number of read bit lines, wherein each read bit line is coupled to the first source/drain regions of the second transistors in a row of vertical pairs in the array; and

forming a number of read wordlines, wherein each read wordline is coupled to the second source/drain regions of the second transistors in a column of vertical pillars in the array;

forming a number of bit line drivers coupled to the respective read and write bit lines; and

forming a number of wordline drivers coupled to the respective read and write wordlines.

19. The method of claim 18, wherein the method further comprises:

forming a number of input/output controls coupled to certain ones of the read and write bit lines and wordlines; and

forming a number of address decoders coupled to the read and write bit lines and wordlines.

20. The method of claim 18, wherein the forming of the number of charge storage nodes includes forming the number of charge storage nodes such that a data state on the charge storage nodes controls an operation of the second transistors.

21. The method of claim 18, wherein the forming of the number of charge storage nodes includes forming a number of plate capacitors.

22. The method of claim 18, wherein the forming of the number of read wordlines comprises forming the number of read wordlines to be buried beneath the second source/drain regions of the second transistors.

23. The method of claim 18, wherein the forming of the number of write wordlines in the memory array comprises forming the number of write wordlines of heavily doped n+ type polysilicon.

24. A method for fabricating a data storage device, the method comprising:

forming a number of vertical pillars forming an array of rows and columns, each vertical pillar having a vertical write transistor and a vertical read transistor each having a body region, a gate region, and first and second source/drain regions;

forming a number of plate capacitors that surrounds each vertical pillar adjacent to the second source/drain region of the write transistor, wherein each plate capacitor is coupled to the second source/drain region of each write transistor in the vertical pillars, and wherein a charge stored on each of the plate capacitors controls a conductivity of each of the read transistors in the vertical pillars;

forming a number of independent read bit lines for nondestructive read operations, wherein each independent read bit line is coupled to the first source/drain regions of the read transistors in one row of the vertical pillars;

forming a number of read wordlines, wherein each read wordline is coupled to the second source/drain regions of the read transistors in one column of the vertical pillars;

forming a read bit line driver coupled to each of the read bit lines;

forming a read wordline driver coupled to each of the read wordlines;

forming a number of input/output controls coupled to certain ones of the read bit lines and wordlines;

forming a read bit line decoder operatively coupled to the read bit line driver; and

forming a read wordline decoder operatively coupled to the read wordline driver.

25. The method of claim 24, wherein the forming of the number of independent read bit lines comprises forming the number of independent read bit lines of heavily doped p+ type polysilicon.